IN THE CLAIMS

Please amend claims 1, 2, 6, 8, 9, 14, and 17 as follows. All claims have been provided as a courtesy to the Examiner.

1. (Twice Amended) A memory module, comprising:

a plurality of memory devices; and

a memory module controller [configured] to receive a first memory transaction in a first format from a first memory bus, and to convert the first memory transaction into a second memory transaction in a second format for the plurality of memory devices, the second format of the second memory transaction being different from the first format of the first memory transaction.

2. (Twice Amended) The memory module of claim 1, wherein the memory module controller is [also configured] to reformat the first memory transaction in the first format into the second memory transaction in the second format, and is to provide the second memory transaction to at least one of the plurality of memory devices.

3. (Unchanged) The memory module of claim 1, further comprising:

a second memory bus coupled between the memory module controller and the plurality of memory devices.

4. (Unchanged) The memory module of claim 3, wherein the second memory bus comprises separate address, data, and control signal lines.

5. (Unchanged) The memory module of claim 3, wherein the second memory bus comprises a signal line for a clock signal.

6. (Twice Amended) The memory module of claim 3, wherein the first memory bus is to operate [operates] at a first data rate and the second memory bus is to operate [operates] at a second data rate, and wherein the first data rate is different than the second data rate.

7. (Unchanged) The memory module of claim 1, wherein the first memory bus includes a first number of signal lines and the second memory bus includes a second number of signal lines, and wherein the first number is different than the second number.

8. (Twice Amended) The memory module of claim 1, wherein the memory module controller comprises:

request handling circuitry [configured] to receive the first memory transaction from the first memory bus; and

control logic coupled to the request handling circuitry and [configured] to reformat the first memory transaction and to provide the reformatted first memory transaction to at least one of the plurality of memory devices.

9. (Twice Amended) The memory module of claim 1, wherein the first memory bus is [configured] to carry time-multiplexed data and address information, and the second memory bus includes separate address and data lines.

10. (Unchanged) The memory module of claim 1, wherein the memory module is a dual in-line first memory module (DIMM).

11. (Unchanged) The memory module of claim 1, wherein the memory module is a single in-line first memory module (SIMM).

12. (Unchanged) The memory module of claim 1, wherein the plurality of memory devices comprise volatile memory devices.

13. (Unchanged) The memory module of claim 1, wherein the plurality of memory devices comprise nonvolatile memory devices.

14. (Twice Amended) The memory module of claim 1, wherein the memory module controller is [configured] to generate a handshake signal that indicates [when] if the memory module controller is communicating data to the system memory controller.

15. (Unchanged) The memory module of claim 1, wherein the first memory transaction is a write transaction.

16. (Unchanged) The memory module of claim 1, wherein the first memory transaction is a read transaction.

17. (Twice Amended) A memory module, comprising:

a plurality of memory devices; and

a memory module controller coupled to the plurality of memory devices, the memory module controller [being configured] to receive a first memory transaction in a first format from a memory bus, and to convert the first memory transaction into a second memory transaction in a second format, and to provide the second memory transaction in the second format to at least one of the plurality of memory devices.